Remarks

Claims 19-23, 27-29, and 31-33 stand rejected and remain pending. Claims 1-18, 24-26, 30, and 34 were canceled in previous responses. No claims are amended herein. The Applicant respectfully traverses the rejection and requests allowance of claims 19-23, 27-29, and 31-33.

Claim Rejection Under 35 U.S.C. §§ 102 and 103

Claims 19-23, 27, 29, 31, and 32 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,272,616 to Fernando et al. (hereinafter "Fernando"). (Page 2 of the final Office action.) Claims 28 and 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fernando in view of U.S. Patent No. 5,303,354 to Higuchi et al. (hereinafter "Higuchi"). (Page 12 of the final Office action.) The Applicant respectfully traverses the rejection in view of the following discussion.

Claims 19 and 31

 A. Throughput Mode

Independent method claim 19 indicates that a bundle of instructions from each of first and second program threads are distributed to a first cluster of execution units for execution, while a bundle from each of third and fourth program threads are distributed to a second cluster of execution units for execution in throughput mode. In other words, during throughput mode, each of the two recited clusters receives instructions from more than one thread. Paragraph [0019] of the present application describes such execution in one embodiment as "maximum throughput of four separate threads." Independent processor claim 31 incorporates similar provisions.

The final Office action indicates that Fernando teaches the throughput mode of claims 19 and 31 by way of its MIMD mode. (Pages 3-7 of the final Office action.) The Applicant respectfully disagrees, as the MIMD mode of Fernando appears to only teach the receipt and execution of instructions from a single program thread or stream at each of the instruction pipelines. For example, Fig. 7, which indicates the use of four instruction pipelines, shows threads 1 through 4 each being executed on separate instruction pipelines while in MIMD mode at times t1 through t9. (See column 11, lines 33-60.) At times t10 through t12, instruction

pipelines 1 and 2 operate in SIMD mode, while instruction pipeline 4 operates in MIMD mode on thread 4. (See column 11, line 60, to column 12, line 4.)

In response, the final Office action asserts that "Applicant's arguments appear to focus on the fact that Fernando's examples of their invention only mention one main program with one fork thread operating per pipeline and insinuating that, since only one main program with one fork thread operating per pipeline is shown in Fernando, there will be only one main program ever run on the device and each pipeline will run only one fork thread." (Page 14 of the final Office action.)

The Applicant respectfully disagrees, as the Applicant made no such assertion. Further, the Applicant respectfully notes that the first through fourth bundles of claims 19 and 31 are from separate threads of *a multiply-threaded program*. In other words, the threads are all from the same program. Thus, even if Fernando begins a second main program with a second group of threads after a first main program with a first group of threads has completed, the first and second group of threads are not part of the same multiply-threaded program, as set forth in claims 19 and 31, since two different main programs are involved.

The final Office action further indicates that times t10 through t12 of Fig. 7 of Fernando show that data path 2, previously used at times t2 through t7 for thread 2, is reused for thread 1 *in SIMD mode*. (Page 14 of the final Office action.) However, since the final Office action also indicates that the SIMD mode disclosed in Fernando teaches the *wide mode* of claims 19 and 31 (pages 7-10 of the final Office action), the use of data path 2 to operate on the data of thread 1 during SIMD mode does not teach or suggest a separate thread being executed on data path 2 during the *throughput mode*, as provided for in claims 19 and 31.

The final Office action further emphasizes that "[t]he exemplary embodiments of Fernando are exactly that, exemplary embodiments. They are meant for simple explanation of how Fernando's system function[s], and not limiting Fernando's system to executing only a single main program and three fork threads on four pipelines." (Pages 14 and 15 of the final Office action.) However, to be a proper 35 U.S.C. § 102(e) reference, Fernando must teach or suggest each provision of the rejected claims. As described in detail above, the Applicant contends that Fernando does not teach or suggest two clusters, each of which receives instruction bundles from two separate program threads while in throughput mode, as provided for in claims 19 and 31, and such indication is respectfully requested.

B. Wide Mode

Claim 19 also indicates that separate bundles of the same thread of a program are fetched and distributed to separate clusters in wide mode. Independent processor claim 31 incorporates similar provisions.

As mentioned above, the final Office action alleges that SIMD mode teaches the wide mode of claims 19 and 31. (Pages 7-10 of the final Office action.) The Applicant respectfully disagrees with the allegation. Fernando indicates that in SIMD mode "*a single instruction is decoded and run through multiple processor pipelines* wherein, in each processor pipeline, it operates on different data sets." (Column 2, lines 15-18; emphasis supplied.) In other words, each instruction is fetched and distributed to each processor taking part in SIMD mode. This operation is further described in Fig. 3, which indicates that a single fetch unit 20*a* of the primary execution pipeline 16 fetches each single instruction, which is sent to, decoded by, and executed by each of the primary execution pipeline 16 and the secondary execution pipeline 18. (See column 6, lines 41-54.) The state diagram of Fig. 5 further emphasizes that in SIMD mode 52 "Side A fetches and executes," while "*Side B executes instruction fetched by Side A*." (Emphasis supplied.) Therefore, each processor in SIMD mode executes the same instructions, albeit on different data sets. The SIMD mode of Fernando thus does not teach or suggest fetching and distributing *different bundles of instructions* from the same thread to different clusters for processing or execution, as provided for in claims 19 and 31, and such indication is respectfully requested.

Claims 20-23, 27-29, 32, and 33

Claims 20-23 and 27-29 depend from independent claim 19, while claims 32 and 33 depend from independent claim 31, thus incorporating the provisions of their respective independent claims. Thus, the Applicant asserts that claims 20-23, 27-29, 32, and 33 are allowable for at least the reasons provided above in support of claims 19 and 31, and such indication is respectfully requested.

Therefore, in light of the foregoing, the Applicant respectfully requests the withdrawal of the 35 U.S.C. §§ 102 and 103 rejections of claims 19-23, 27-29, and 31-33.

<u>Conclusion</u>

Based on the above remarks, the Applicant submits that claims 19-23, 27-29, and 31-33 are allowable. Additional reasons in support of patentability exist, but such reasons are omitted in the interests of clarity and brevity. The Applicant thus respectfully requests allowance of claims 19-23, 27-29, and 31-33.

The Applicant believes no fees are due with respect to this filing. However, should the Office determine additional fees are necessary, the Office is hereby authorized to charge Deposit Account No. 08-2025 accordingly.

Respectfully submitted,

Date: <u>11/16/2007</u>

<u>/Kyle J. Way/</u>

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